Exhibit "A"

nvention disclosure submission Complete all sections and send to the Nortel-Patent Dept structure of TTAWA, Canada: Patent Ocpt., 0265, NTPAT		-8t/	No. TW0007	NØRTE I	
or HARLOW, UK: Pater or RICHARDSON, USA	nt Dept., HALQ5		RICHI	Attny/Agent	
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Name usually known Norbert	88:				
Global ID					
Phone	Location WINNIPE	Department CPE	Mailstop n/a	Occupation	Fax
Signature		Date		Citizen of CANADA	
(2) Name of supervisor	or divisional head			(5) Project Number	
Bernard Brown			3	n/a	
lome of AVP Reported t Doug Smith	o:			(6) Indicate your LOB Wireless Networks	
Signature		Date		If Advanced Technology, please indicate which group. Please Make a Selection	
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3) Date of first written d	escription.			Key words for searching	
las this Invention been d	iscussed with othe	rs? If so, please	complete.		
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When? Was there a Non-Disclosure Agreement in place?				Are you aware of any imm	ilnent future disclosures? Please detail.
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1) Which products will u	se this invention?	L		(7) Is the invention releva	ant to a Standards activity?
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	FECTIVICAL INFORMATION	
Brief description of the invention		
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Page 2

TECHNICAL INFORMATION (continued)

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(1) Full legal name of firs	st inventor (incl	ude middle initia))	Residence address (and	post office address if different)
Wegner Norbert - Global ID					
Phone	Location		t Mailstop	Occupation	Fax
Signature		Dat	e	Citizen of CANADA	
Contractor Information				Any other agreement(s) wit	n your agency.
Agency worked for Non disclosure agreement with Nortel				Please specify	
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1) Full legal name of 2nd	inventor (includ	le middle initial)			post office address if different)
Peter A.	Me cath	ached	tbd	To be sent later	
Phone	Location WINNIPE	Department NNE	Mailstop n/a	Occupation	Fax
Signature		Date		Citizen of UKRAINE	
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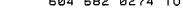
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Sending ATM Cells Across PCI to PCI Bridges With Small Buffers From The Secondary to Primary Side

Problem:

Nortel -BWA is using the PCI bus as a medium to transfer ATM cells between cards in a chassis based Compact PCI product. Since the Compact PCI bus is limited to 8 loads per bus segment PCI to PCI bridges are used to extend the number of slots that can be supported in a single chassis. In order to maximize the bandwidth of the PCI bus, all cards in the system transfer their outgoing ATM cells by performing a write burst of a 14 Dword ATM cell to a preprogrammed target address. Using writes to transfer data allows write posting across PCI to PCI bridges which maximizes bandwidth utilization. If the target address is on a different bus segment than the initiator, the burst will be write posted into the bridge's buffer. If an initiator is bursting an ATM cell across the bridge and the bridge buffer fills up, then the bridge will do a target disconnect even if the ATM cell has not been completely transferred. The arbiter will grant the bus to the next initiator which will write a complete ATM cell over top of the partial ATM cell that is already in the buffer. The initiator that was disconnected will finish sending its ATM cell when it is next granted the bus. If all of the cells crossing the bridge were to the same target address, the cells will be corrupted when they arrive at the target because of the disconnect that happened while crossing the bridge.

Certain cards in the system, such as modems and cell multiplexers, will have multiple cards writing to a single FIFO target location on that card. In order for these cards to operate properly the 14 DWord bursts must be written into the FIFO as complete cells and not as partial cells. i.e. the ATM cells must arrive in their entirety and not be broken up.

A summary of the problem is that target disconnects must be prevented when data from multiple initiators intended for a single target address crosses a PCI to PCI bridge to ensure that ATM cells arrive intact:

Solution:

The CPCI architecture is as shown in figure 1. Arbitration on Bus 1 is controlled by the Host to PCI bridge that physically resides on the host CPU. Arbitration on Busses 2 and 3 is controlled by the PCI to PCI bridge connected to them. The following assumptions are made when using this architecture:

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 initiators must never cause a "target disconnect with data" when being written to. "Target
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Based on these assumptions, disconnects must only be prevented when data is being written from busses 2 or 3 to bus 1. This is because disconnects are only a problem when multiple initiators are writing to a single target which by definition is on bus 1.

Disconnects on busses 2 and 3 are avoided by preventing any of the cards on the secondary bus from being granted the bus when there isn't enough room in the bridge buffer for a complete ATM cell. A counter exists on the PCI to PCI bridge module that is incremented when a card on its secondary side starts a write transaction to the bridge. The write may be a single word or a multi DWord burst and will be referred to a data unit. The counter is decremented when the bridge successfully completes a write transaction on its primary side. The counter is not decremented if the bridge gets a target disconnect since this indicates that the data unit was not completely sent. If the counter value is equal to the maximum number of data units that the secondary to primary buffer on the bridge can hold, then the arbitration on the secondary bus is parked and the bus is granted to the bridge whether it is requesting or not. Arbitration is not affected when the count value is less than this maximum value. The size of the data unit is assumed to the maximum size of a burst which is 14 DWords.

<u>Bus</u>

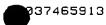
PCI



Counting data units requires only a small counter and thus minimal hardware resources. The limitation to this method is that it assumes that all data units are the same size, which is generally the case. If the size of the data units varies, the buffer is inefficiently utilized. If the size of the data units varies an extension of this method is to count DWords instead of data units and to disable the grants to the secondary bus if there is not enough room for the maximum size of a burst. This requires more hardware to implement.

Figure 1 - Nortel - BWA Compact PCI Architecture

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Received from < 604 682 0274 > at 3/18/03 4:35:43 PM [Eastern Standard Time]-

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TW0007 No. Rec'd.

Attny/Agent

17 Mar 98



Invention Title Method for Sending ATM Cells Across PCI to PCI Bridges With Small Buffers From The Secondary to Primary Side Correspondence will be directed to the first-named inventor only. Residence and post office address if different (1) Full legal name of first inventor (include middle initial) Wegner Norbert Name usually known as: Norbert Global ID Fax Location Department Mailstop Occupation Phone WINNIPE CPE n/a Date Signature Citizen of CANADA (5) Project Number (2) Name of supervisor or divisional head Bernard Brown Name of AVP Reported to: (6) Indicate your LOB Doug Smith Wireless Networks Date Signature If Advanced Technology, please indicate which group. Please Make a Selection Technical field Key words for searching (3) Date of first written description. Has this invention been discussed with others? If so, please complete. **Qutside Nortel** To Whom? When? Are you aware of any imminent future disclosures? Please detail Was there a Non-Disclosure Agreement in place? Inside Nortel To Whom? When? (7) Is the invention relevant to a Standards activity? (4) Which products will use this invention? If so give details: (8) Does this invention arise from any arrangement, involving any external organization? no Organization Contract no.

•	TECHNICAL INFORMATION	No. TWO
a) Brief description of the Invention		
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TECHNICAL INFORMATION (continued)

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Additional Inventors / Contractor Information

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No. TW000

(1) Full legal name of first inventor (include middle (nitial)				Residence address (and post office address if different)		
Wegner	Norbert					
Globel ID						
						
Phone	Location WINNIPEC		nt Mailsto n/a	Occupation	Fax	
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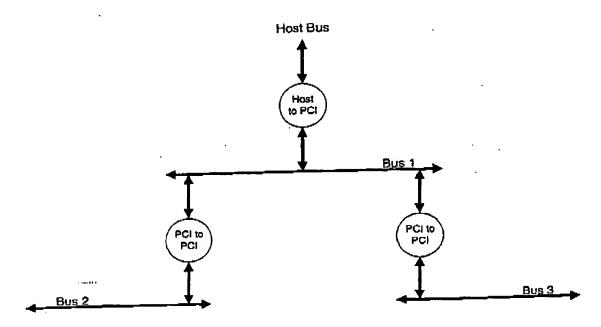


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